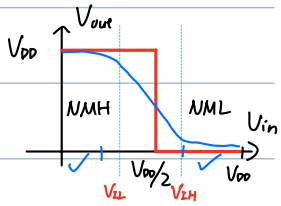
Digital

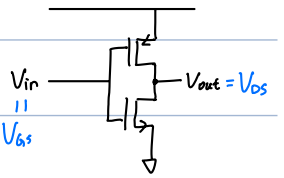
Inverter (ideal) ideality based on suppression on noise/error



E. chain $V_{in} = \varepsilon \xrightarrow{\to 0}$ ▷ ▷ ▷ V_{o3}

E. extremely nonideal (slope = -1 curve) → $V_{o3} = V_{DD} - \varepsilon$ → not suppressed :(

slope = -1 → V_{IH}, V_{IL} → H/L suppressed.



CMOS $V_{DD} - V_{IH} = NMH$, $V_{IL} - 0 = NML$

TTL $V_{max} \neq V_{DD}$, $V_{min} \neq 0$

▷ 1. p sat $i_d =$ n triode (not yet

$$\frac{1}{2}k'\left(\frac{W}{L}\right)_p \left(\overbrace{V_{DD}-V_{in}}^{V_{sg}} - V_{Tp}\right)^2 = i_{dp} = i_{dn} = k'\left(\frac{W}{L}\right)_n \left(\overbrace{V_{in}}^{V_{gs}} - V_{Tn} - \frac{1}{2}\overbrace{V_{out}}^{V_{ds}}\right)\overbrace{V_{out}}^{V_{ds}}$$

2. $\frac{\partial V_{out}}{\partial V_{in}} = -1$

3. set $V_{in} = V_{IH}$ → solve for V_{out}

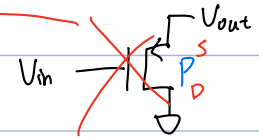
4. plug back to 1.

	N	P
	cutoff	linear
V_{IL} →	sat	lin/tri
	sat	sat
V_{IH} →	tri/lin	sat
	lin	cut

if PMOS used to pull down, can't continue beyond V_{Tp}

present drain side to output, if source side → ~ src follower, X

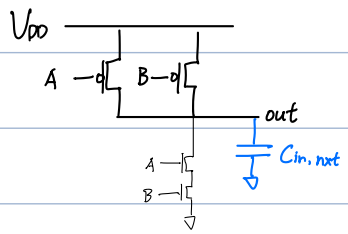
E. if flip I/O, and P/N, won't work → source follower, noninverting



AND need pull down on 0 if any input is 0 → PMOS only → X

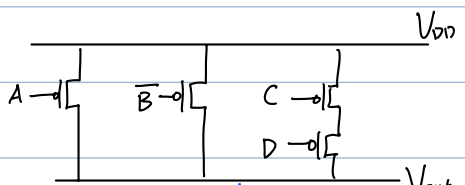
NAND up on 0 → PMOS pullup → ✓ ▷○ AND

down on both 1 → NMOS pulldown



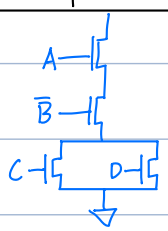
NOR

custom pullup (SoP)

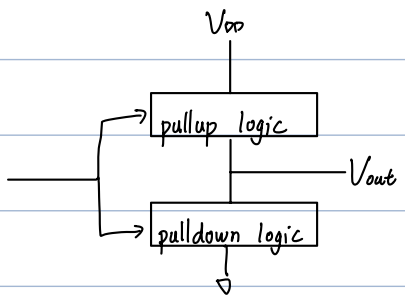


$Y = \overline{A\bar{B}(C+D)} = \bar{A} + B + \bar{C}\,\bar{D}$

pulldown

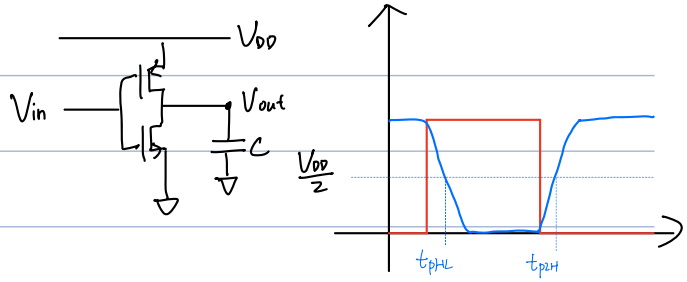


$\bar{Y} = A\bar{B}(C+D)$



Delay prop T_{pLH} T_{pHL}, 50%

$T_p \propto \frac{C}{k'\frac{W}{L} V_{DD}}$ for long channel

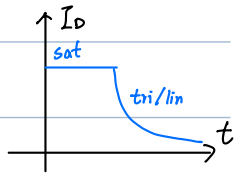


$k'\frac{W}{L} \propto I_D$ (all regions)

sat $I_D = \frac{1}{2} k'\frac{W}{L} (V_{DD} - V_T)^2$

tri $= k'\frac{W}{L} (V_{DD} - V_T - \frac{V_{SD}}{2})^2$

lin $= V k'\frac{W}{L} (V_{DD} - V_T)$



V_{DD}

lin. $V_{out} = V_{DD}(1 - e^{-t/RC})$ $e^{-1/R}$ outweighs V_{DD}

$C \propto wL \rightarrow$ reduce L

Short-channel → sat → assume resistive pull up/down

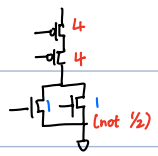
E. pulldown → PMOS off, NMOS → R_N → $V_{out}(t) = V_{DD} e^{-t/R_N C}$

(50%) $T_{pHL} \approx \ln 2 \, R_N C$, R_N is emperical

symmetry $(k'\frac{W}{L})_n$ and $(k'\frac{W}{L})_p$ (typically $k'_n > k'_p$, need make p wider)

series, looks like $\frac{W}{2L}$ → slower :(→ need double widths } worst case

parallel $\frac{2W}{L}$ → faster, but worst case same }

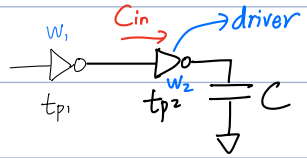
E. NOR 

$k'_n = 2k'_p$

↳ 10 units

E. NAND 2 units for N, 2 for P → 8 units → smaller!

D^o drives an off-chip C ($>> C_{gs}, C_{gd}$), $t_{p2} = \frac{C}{k'\frac{W_2}{L} V_{DD}}$

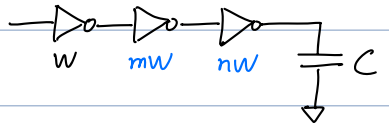


$C_{in2} \propto W_2 L$ is large, since $(\frac{W}{L})_2$ is large $t_{p1} = \frac{C_{in2}}{k'\frac{W_1}{L} V_{DD}}$

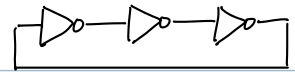
$(\frac{W}{L})_1$ need large → L typ. fixed, W↑

$t_{pA} \propto \frac{mwL}{k'\frac{W}{L} V_{DD}}$ $t_{pB} \propto \frac{nwL}{k'\frac{mW}{L} V_{DD}}$

$t_{pA} + t_{pB} \propto \frac{L^2}{k' V_{DD}} (m + \frac{n}{m}) \rightarrow m = \sqrt{n}$ at min delay

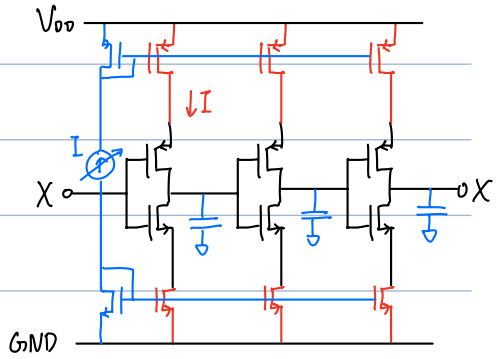


Oscillator $T = 2 \cdot 3\, t_d = 6 t_d$



Phase lock loop (PLL) match TX/RX phase

limit (starve) gate current, set I ↗ mirror, so T match

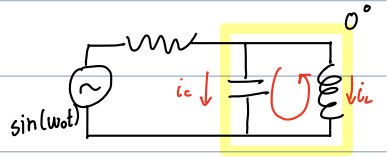


Single ▷o

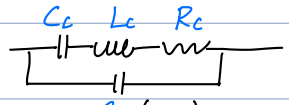
$Z_{LC} \overset{\cdots}{=} \frac{jwL}{1-w^2LC}$, ∞ if $w_0 = \frac{1}{\sqrt{LC}}$

$i_C = C\frac{dv}{dt} = Cw_0\cos(w_0 t) = \sqrt{\frac{C}{L}}\cos(w_0 t)$

$i_L = \frac{1}{L}\int v\,dt \quad \overset{\cdots}{=} -\sqrt{\frac{C}{L}}\cos(w_0 t)$

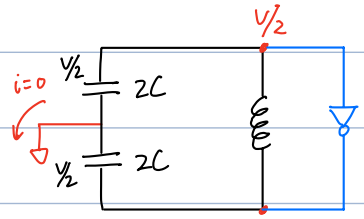


XTAL Crystal ⊣⊢

$Z_{crystal} = $ 

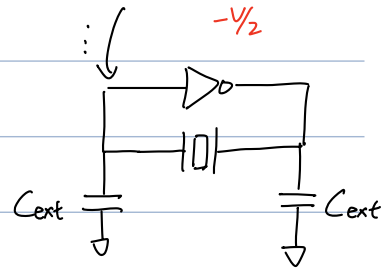
$\overset{\cdots}{=} \frac{j}{w}\frac{w^2LcCc-1}{(Co+Cc)-w^2LcCcCo}$ sharper

can be made ∞ (parallel res.) or 0 (series res.)



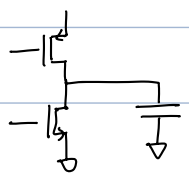
parallel $f_{parallel} \overset{\cdots}{=} \frac{1}{2\pi\sqrt{LcCc}}\sqrt{1+\frac{Cc}{Co}} \approx \frac{1}{2\pi\sqrt{LcCc}}$

if external caps added, $\hookrightarrow = 1$ if $Co >> Cc$



▷o is positive feedback supply

CMOS power no continuous power



Transition (driving a C) N $1 \to 0$: C's energy $\frac{1}{2}CV_{DD}^2$ dissi from Q

P $0 \to 1$ $P_Q = I_D V_{SD} = I_D(V_{DD} - v_C)$

$p_Q(t) = C\frac{dv_C}{dt}(V_{DD} - v_C)$

$W = \int_0^\infty p(t)\,dt$

$= \int_0^{V_{DD}} C(V_{DD} - v_C)\,dv_C = \frac{1}{2}CV_{DD}^2$

Total: $CV_{DD}^2 \rightarrow p = f_{activity} C V_{DD}^2$

E. Apple M4, 4GHz (x 1/500), 28G transistors (x 1/4), C = 1fF, V_{DD} = 0.9V

$\frac{4E9}{500} \times 1E{-}15 \times 0.9^2 \times \frac{28E9}{4} = 45\,W$

if P/N both on → $I_{crowbar}$ → want low (sharp waveform)

(assume matching $(k'\frac{W}{L})_{p,n}$)

typically ignored

avoid staying near $V_{DD}/2$

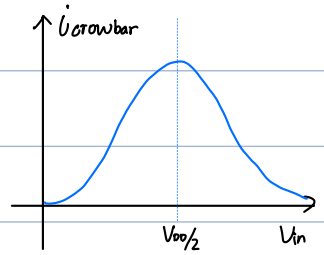
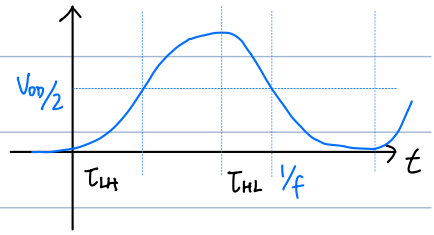
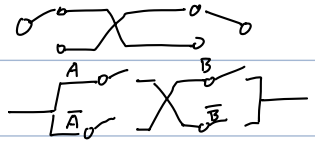


Figure of merit : power-delay product $= fC V_{DD}^2$ (I) $t_p = \frac{1}{2} C V_{DD}^2$ (avg)

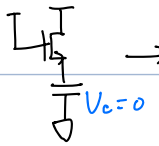
E. clk an ▷o to the fastest $t_p = \frac{1}{2}(\tau_{LH} + \tau_{HL}) \approx \frac{1}{2} \frac{1}{f}$



Pass-transistor (sw) Logic E. XOR switch



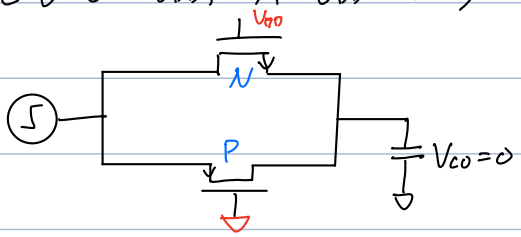
N → source follower → (pullup) max : $V_{DD} - V_T$



pulldown ✓ if $V_D = 0$, $V_C = V_{DD}$ (symmetrical)

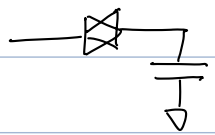
P oppo (✓ $0 \to V_{DD}$, ✗ $V_{DD} \to 0$) ⇒ CMOS

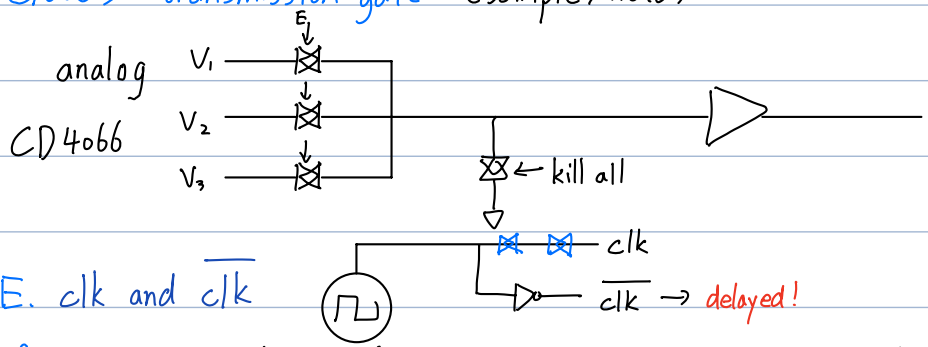
CMOS sw



For rising, when N fails, P takes over

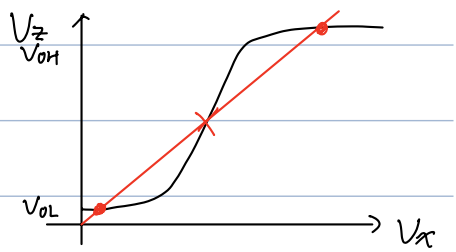
CMOS transmission gate (sample/hold)



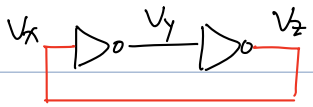


E. clk and $\overline{clk}$

fix : buffer clk w/ trans. gates → passive delay



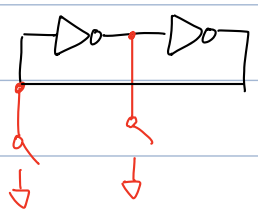
Bistable



Delay : ∫ curve

Loadline : $V_X = V_Z$

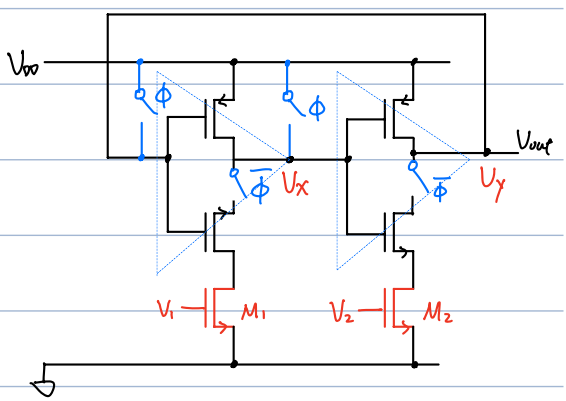
→ (static) SRAM, fast, 4Q + 2SW = 6 how to set ?



1. Brute force : switch V_X / V_Y to 0

(crowbar current while switching)

2. clked comparator clk: ϕ

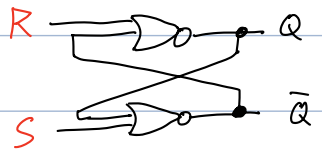


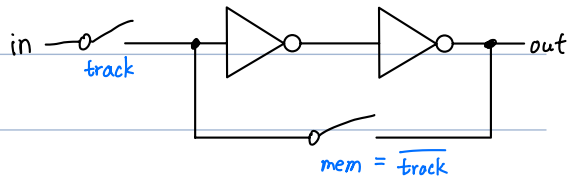
M_1, M_2 current-starve pulldown.

if $V_1 > V_2$, $V_X \to 0$ foster than $V_Y \to$ pos. feedback

SR

	S	R	Q(t+1)	$\bar{Q}(t+1)$
set	1	0	1	0
res	0	1	0	1
hold	0	0	Q(t)	$\bar{Q}(t)$
invalid	1	1	0	0

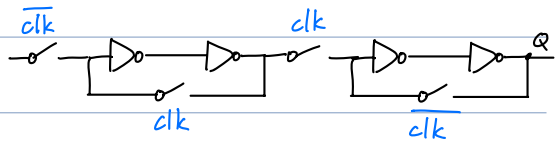




Dynamic gates track / hold

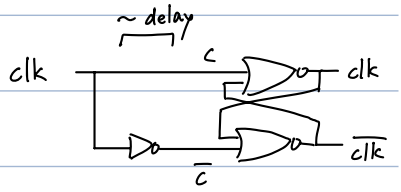
DFF updated at CLK rising edge ⎍

Master-slave Take turns track & hold

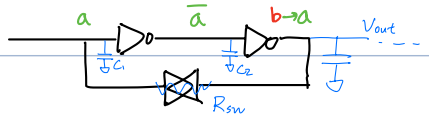


Non-overlapping clk, $\overline{clk}$ → ~SR latch ensures not both high

If inputs both high → both outputs 0

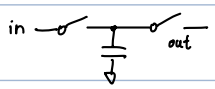


Latch



wants to overwrite b→a, b needs to drive $C_{in,next}$ and $R_{sw}C_1$ → slower than charging C_2, a wins

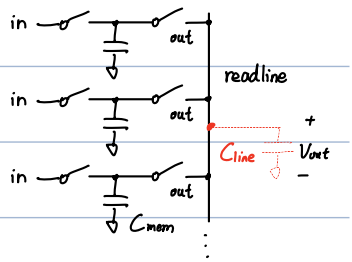
dynamic DRAM (sample-hold)



long readline → huge C_{line} >> C_{mem}

Store $Q = C_{mem} V_{DD}$

Recall Charge C_{line} starts w/ $\frac{V_{DD}}{2}$



$V_{out} = \frac{V_{DD}}{2}\frac{C_{line}}{C_{mem}+C_{line}}$ if $C_{mem}=1$; $\frac{V_{DD}}{2}\left(\frac{C_{line}+2C_{mem}}{C_{mem}+C_{line}}\right)$ if $C_{mem}=0$

Make a sensitive comparator (so DRAM slower than SRAM)

1. precharge readlines B and $\bar{B}$ to $\frac{V_{DD}}{2}$
2. select cell. B / $\bar{B}$ will shift slightly
3. Diff. amp when latch turned on $\xrightarrow[\text{feedback}]{\text{pos}}$ saturates

CLK recovery TX clk match & sync w/ RX clock, RX sample w/i a period!

1. Avoid consecutive 0/1s in encoding

   E. alphabet: 26 ≤ 5-bits (32) → avoid 00000 11111 01111 10000 0000| 1111|0

2. extract clk from data

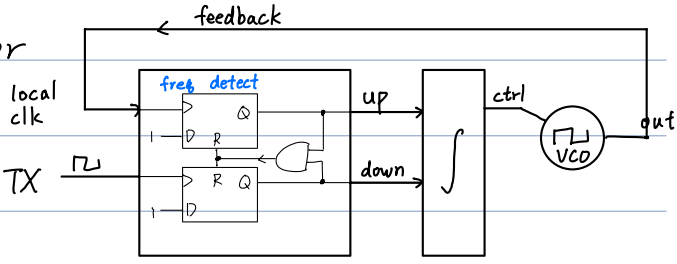
   ① rough tuning of local clk (TX clk): TX sends oscillating 1/0 → compare TX/local clk counter

   Coarse adjust local clk (change $\frac{1}{T}$, D0, etc.)

   ② Fine tuning (lock f): voltage-controlled oscillator

   TX still oscillates 1/0

   first CLK sets DFF → up/down → reset DFF



3. Lock the phase TX sends data

   sample a,b,c from local clk → 2 dff for a, c, 1 for b

   if a=b ≠ c → early → down pulse up = $\bar{a}bc + a\bar{b}\bar{c}$

   a≠b=c → late → up pulse down = $ab\bar{c} + \bar{a}\bar{b}c$

   a=b=c → no change

   a≠b≠c → error → nothing